



**UNITED STATES DEPARTMENT OF COMMERCE**  
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
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09/320,421 05/26/99 FORBES

L 303.586US1

021186 MM91/0426  
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EXAMINER

TRA, A  
ART UNIT

PAPER NUMBER

2816  
DATE MAILED:

04/26/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trad marks

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**Advisory Action**

Application No.

09/320,421

Applicant(s)

FORBES ET AL.

Examiner

Art Unit

Quan Tra

2816

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 16 April 2001 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE. Therefore, further action by the applicant is required to avoid abandonment of this application. A proper reply to a final rejection under 37 CFR 1.113 may only be either: (1) a timely filed amendment which places the application in condition for allowance; (2) a timely filed Notice of Appeal (with appeal fee); or (3) a timely filed Request for Continued Examination (RCE) in compliance with 37 CFR 1.114.

**PERIOD FOR REPLY** [check only a) or b)]

- a) ☒ The period for reply expires 3 months from the mailing date of the final rejection.
- b) ☐ In view of the early submission of the proposed reply (within two months as set forth in MPEP § 706.07 (f)), the period for reply expires on the mailing date of this Advisory Action, OR continues to run from the mailing date of the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

1. ☐ A Notice of Appeal was filed on \_\_\_\_\_. Appellant's Brief must be filed within the period set forth in 37 CFR 1.192(a), or any extension thereof (37CFR 1.191(d)), to avoid dismissal of the appeal.
2. ☐ The proposed amendment(s) will be entered upon the timely submission of a Notice of Appeal and Appeal Brief with requisite fees.
3. ☒ The proposed amendment(s) will not be entered because:
- (a) ☒ they raise new issues that would require further consideration and/or search. (see NOTE below);
- (b) ☐ they raise the issue of new matter. (see Note below);
- (c) ☒ they are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
- (d) ☐ they present additional claims without canceling a corresponding number of finally rejected claims.

NOTE: See Continuation Sheet.

4. ☐ Applicant's reply has overcome the following rejection(s): \_\_\_\_\_.
5. ☐ Newly proposed or amended claim(s) \_\_\_\_\_ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
6. ☒ The a) ☐ affidavit, b) ☐ exhibit, or c) ☒ request for reconsideration has been considered but does NOT place the application in condition for allowance because: See Continuation Sheet.
7. ☐ The affidavit or exhibit will NOT be considered because it is not directed SOLELY to issues which were newly raised by the Examiner in the final rejection.
8. ☒ For purposes of Appeal, the status of the claim(s) is as follows (see attached written explanation, if any):
- Claim(s) allowed: \_\_\_\_\_.
- Claim(s) objected to: \_\_\_\_\_.
- Claim(s) rejected: 1-45.
- Claim(s) withdrawn from consideration: \_\_\_\_\_.
9. ☐ The proposed drawing correction filed on \_\_\_\_\_ a) ☐ has b) ☐ has not been approved by the Examiner.
10. ☐ Note the attached Information Disclosure Statement(s) (PTO-1449) Paper No(s). \_\_\_\_\_.
11. ☐ Other:

*Terry D. Cunningham*  
Terry D. Cunningham  
Primary Examiner

Continuation of 3. NOTE: The drain region for the pair of transistors in each inverter is coupled to a drain region of the transistor of the first conductivity type in the same inverter, is coupled directly to the gate of the transistor of the first conductivity type in the other inverter.

Continuation of 6. does NOT place the application in condition for allowance because: The specification fails to teach dual-gate transistor is a combination of two parallel connected transistors having a share body region. Therefore, any unit having two gates can be considered as "dual gate". The 6104068 reference is patented after the present invention. Therefore, the dual gate transistor which is a combination of two parallel transistors having a share body region is not well known in the art at the time of the invention. .